XEROX
BUSINESS SYSTEMS
Systems Development Department

To: SDD

Date: August 10, 1979

From: Bob Belleville

Org: SDD/SD&T Workstation Design

Subject: **Dandelion - Function and Performance**

Filed: [Iris]<Workstation>Public>dandelion-fp.memo

c: SDD Managers and concerned staff

The purpose of this memo is to describe, in bullet form, all the functional and performance characteristics of the Dandelion design which Workstation Design thinks may have an impact on the Star product or its development.

Warning

If you are a future user of the Dandelion based Star Workstation you should sit down right now and read this memo all the way through.

Point of Contact

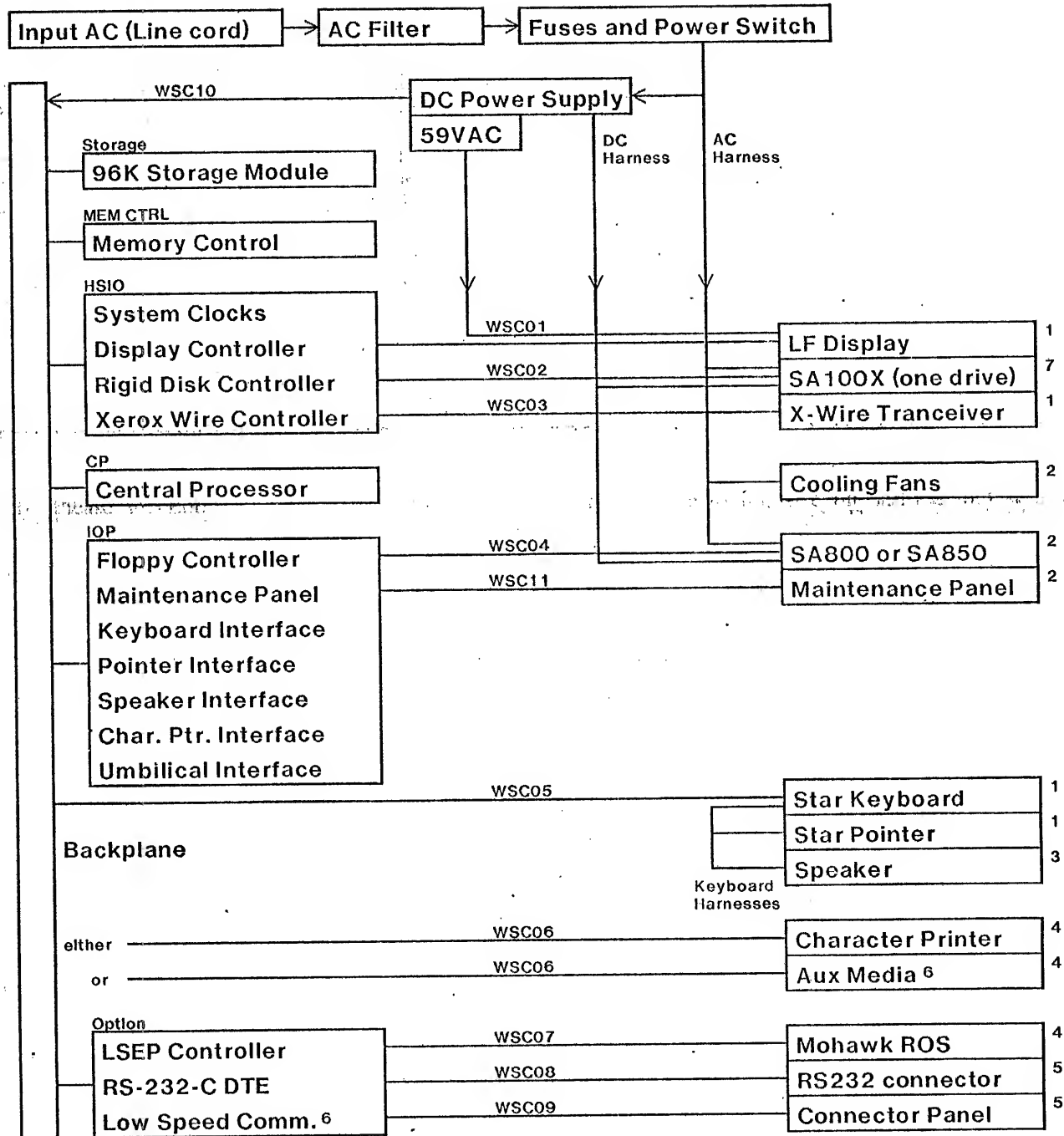All questions may be directed to R. Belleville (8*923-4520) (SDD Palo Alto).

Configuration

The figure on the next page shows the baseline configuration of the Star Workstation. This is the only configuration of the machine planned for Star 1.

O No remote or computer controlled power up or down is included. There is a mechanical, rocker-type, power switch on the front of the console under a cover.

O There is no provision for power fail detect - the machine will simply crash. With the exception of a disk sector actually being written during the failure, disk media will not be damaged.

O Two momentary contact pushbuttons are included with a 4 digit maintenance panel under the cover with the power switch at the front of the machine. One of the buttons (boot) is hardwired to the 8085's reset line. If you push boot, the 8085 has no choice but to boot the machine in a "standard way." If the second button (alternate boot) is held down while boot is pushed, the 8085 will slowly display a sequence of numbers in the maintenance panel which refer to alternate booting strategys. When the user releases the alt. boot button the selected strategy will take place. Note that when the power is turned on the standard boot takes place without the need to push any buttons.

Workstation Configuration   **Base Line Workstation**

| Input AC (Line cord) | → | AC Filter | → | Fuses and Power Switch |

WSC10 ← **DC Power Supply**

59VAC   DC Harness   AC Harness

Storage
96K Storage Module

MEM CTRL
Memory Control

HSIO
System Clocks
Display Controller
Rigid Disk Controller
Xerox Wire Controller

WSC01 — LF Display — 1
WSC02 — SA100X (one drive) — 7
WSC03 — X-Wire Tranceiver — 1

CP
Central Processor

Cooling Fans — 2

IOP
Floppy Controller
Maintenance Panel
Keyboard Interface
Pointer Interface
Speaker Interface
Char. Ptr. Interface
Umbilical Interface

WSC04 — SA800 or SA850 — 2
WSC11 — Maintenance Panel — 2

WSC05 — Star Keyboard — 1
— Star Pointer — 1
— Speaker — 3

Backplane

Keyboard Harnesses

either — WSC06 — Character Printer — 4
or — WSC06 — Aux Media [6] — 4

Option
LSEP Controller
RS-232-C DTE
Low Speed Comm. [6]

WSC07 — Mohawk ROS — 4
WSC08 — RS232 connector — 5
WSC09 — Connector Panel — 5

Notes:

1. Separate housing, power from workstation.
2. Housed within workstation console.
3. Housed within keyboard housing.
4. Separate housing, independent power supply.
5. External connector system (TBD).
6. Not in current development plan.
7. May be replaced by a SA400X disk (one drive only) housed in the modesty panel.

August 1, 1979   RLB
ws-config.sil

Memory

O Implements a 22-bit virtual address space, and 18-bit real address space with room for expansion to 19-bits (512K words).

O The early Dandelion systems will use 16K dynamic RAM parts to implement the memory system. Later systems will use 64K parts. The major restriction with the 16K design is that the size of the total memory is limited to 160K words. Please note that 51K is used for the display bitmap and 16K are needed for the memory map. The 13K of memory remaining in the display's bank cannot be the source or destination for rigid disk, Xerox wire, or IOP transfers (except when the display is off - see below), nor can it be used for the storage of the map. Because the display processor is accessing its memory bank a significant fraction of the time, the speed of memory access to the display bank is about 70% slower than the rest of memory.

O The memory is fully corrected for single bit errors. In fact, the normal microcode will not even detect the fact that a single bit correction has taken place.

O Diagnostic microcode can read and write all the 22 bits of each memory word to diagnose problems.   (16 bits of data 6 of error correction/detection)

O Double bit errors are detected. Double bit errors caused by the emulator cause a trap. Mesa code determines what to do with all double bit errors. No information other than the fact that an error happened in a specific task is recorded.

O The memory bank connected to the display may not be used as the source or destination for rigid disk, Xerox wire, or IOP transfers while the display is running. When the display is "off" the display memory is no different from the rest of main memory.

O Emulator level microcode can address any memory location in the system with no special consideration for the display. If the emulator and the display conflict, the emulator click is aborted and restarted in the next available click by Dandelion hardware. There are worst case conditions when the emulator may be locked out for rather long times when all the I/O devices are running at once; however, these are rare from a statistical point of view.

Display

O The display has 1024 wide by 809 high active dots in the bitmap. A border of several bits surrounds the the active area. The pattern can be any grey value that repeats in a multiple of 8 bits horizontally and every 2 pairs of lines vertically There are 2 8-bit registers, the first is used when the scan line is an even multiple of 2 and the other when odd. (such a pattern is "office talk stipple")

O The display is refreshed approximately 38 times a second. The phosphor is P40 which is a long persistance white. (Used in most of our Altos) The tube is oriented horizontally.

O The display controller maintains the display with minimum impact to the Dandelion microprocessor (unlike D0 or Alto). Hardware to assist in the maintenance of a cursor is provided; however, it is by no means as complete as the Alto's cursor hardware.

O Hardware to support the scrolling of a window is the same as the cursor hardware. The display controller allows the redirection of the word stream from the display memory bank to the display at least twice during a horizontal scan. The ability to write microcode to support the scrolling of a window containing the cursor is in serious doubt.

O Display task microcode also does memory refresh and the maintenance of a 32-bit high speed timer with about 28.8 microsecond resolution (the horizontal line rate).

O The display can be turned off so that it doesn't access memory anymore. The screen can be made all white, all black or all background during this state. If the cursor is on, that is the same as the display being on as far as display bank memory restrictions are concerned. When the display is off the display memory bank is indistinguishable from the rest of memory in speed and accessability.

Central Processor

O The CP is a "Princops capable" microporcessor implemented with 2901 bit-slice cpu parts.

O It has a 3-byte mesa instruction buffer to enhance emulator performance.

O A PROM checks the stackpointer for out of range and causes a trap if there is an error. The stack is limited to a maximum of 14 words.

O A PROM checks for virtual address out of range (>22-bits) and cause a trap on error.

O There are facilities for breakpointing microinstructions.

O The control store is limited to 4K x 48 bits and is readable and writable via the IOP (see below). Parity is checked on each control store read. If there is an error, a register is set and a trap is caused. Of course, if the control store is really out to lunch the machine will soon die.

O There is some hardware to improve bit-shifting, but it is not fully general. Please see Bob Garner or Don Charnley to understand the full implementation details.

Rigid Disk

O Dandelion can have either one SA100X or one SA400X drive at any one time. At present it looks like we can jumper to convert from SA100X to SA400X configuration; however, it is still possible that we will need two different electronic modules.

O There are no provisions for multiple drives.

O There are no provisions for the drives to be outside the console (or modesty panel in the case of the SA400X).

Xerox Wire

O There is nothing particularly unusual about the Xerox wire system on Dandelion.

O There is no provision for the customer to disconnect the tranceiver from the workstation. The connector is inside the cabinet and must be removed by field service.

O There will be no time domain reflectometer (TDR) in this design (13 chips required).

Input/Output Processor (IOP)

O The IOP is an Intel 8085 based processor within Dandelion which services "low" speed I/O devices and serves to boot the central processor, read and write the CP control store and Task Program Counters.

O Standard devices connected to the IOP are: central processor control (booting) and control store read/write; central processor communication port (8 bit input and output plus control); IBM compatible floppy disk controller for both single and double density and double sided diskettes; Star (Level 4) Keyboard interface, mouse interface, simple tone generator to drive a speaker to emulate a bell; character printer interface (RS-232-C DCE) which will also connect to serial aux. media; maintenance panel interface (the day-time clock is actually on the maintenance panel and operates through this interface).

O A battery backed up, day-time clock will be included to count seconds in a 32 bit register which can be set or read by the 8085 processor. The accuracy will be no better than ± a few seconds a month. No other low speed clock hardware is included. The high speed mesa/pilot timers are implemented in microcode. The minimum period is about 28 microseconds.

O Provision has been made for all standard IOP's to have a socket position into which an Alto umbilical system can be hooked. (Costs no logic.)

O Communication between the IOP and the CP is either in byte by byte (relatively slow) mode or via a 8085 DMA transfer. DMA transfers happen at about one byte per 2 microseconds. CP microcode for the IOP port does very little and the bulk of the work happens either in the 8085 or the mesa code in the CP.

O The 8085's RAM memory (perhaps 8K bytes) provides enough buffer to account for considerable latency on the part of Pilot or client programs.

O The RS-232-C DTE interface is an option contained on a separate module. This interface will handle asynchronous, byte-synchronous, and bit-synchronous communication protocols.

O The Low Speed Communication system (alias 8 digital terminals) is not in the Star 1 plan. We are now considering more cost effective solutions to this problem.

O The standard floppy disk implements the following formats:

Single density (1 or 2 sides)

Sector Size (Bytes)	Sectors/Track	(77 tracks in all cases)
128	26	-- IBM 3740 format (very common usage)
256	15	
512	8	

Double density (1 or 2 sides)

Sector Size (Bytes)	Sectors/Track	(77 tracks in all cases)
256	26	-- IBM System 34 format
512	15	
1024	8	

Although the hardware affords us all this flexibility, it is expensive in terms of software in the IOP (and everywhere else for that matter) to fully support all modes at the same time. We should select the minimum numbers of formats we need. To the extent possible, we should stick to the IBM standards which are in wide use throughout the industry.

O Troy format is a potential option; however, it is not planned for Star 1.

O CP microcode to start booting the machine is stored in the 8085's PROMs and is loaded by the 8085 according to the booting strategy programmed into the 8085 program which is also stored in PROM. Additional microcode for either processor can be gotten from any device attached to the system (from the hardware's point of view, of course, there has to be software and file system convensions to support this).

O The machine serial number is stored in the 8085's PROMs and is available to the CP at all times.

Low Speed Electronic Printer (LSEP)

O The LSEP controller is a hybrid which sends page images to the LSEP using both the 8085 and the CP. "Video" is sent with a simple interface which is controlled by special purpose microcode. Engine controls and diagnostics are communicated through a serial connection to the IOP.

O The LSEP controller uses both the display's click and its main memory so they cannot run at the same time. When the LSEP is running, high speed timer maintenance and memory refresh are the responsibility of the LSEP microcode.

Dandelion Microcode

O Dandelion executes a complete microinstruction in 137 ns. (The D0 needs between 180 and 220 ns. depending on the clock rate 90 to 110 ns.) We have been very careful in designing the machine to meet this clock rate. Due to the close interaction between the I/O and the microprocessor, we must meet this rate.

O Fast mesa byte codes (LLn, SLn, ADD for example) execute in 1 click (412 ns.).

O Because the microinstruction rate is faster than the D0 and because the display does not take any appreciable fraction of processor cycles, we have guarded optimism that the machine will be faster than the D0 or Alto.

O Our experience in writing microcode for the mesa emulator indicates the the number of microinstructions for a given function are about the same for the D0 and Dandelion (with perhaps 5% more on Dandelion). Microcode controller sizes for the I/O devices are less than with the D0. I/O devices connected to the IOP are handled by the 8085 and the resulting data is passed through a thin layer of CP microcode to various mesa faces. Given a fixed configuration for the workstation, we feel comfortable with the control store budget of 4K.

O LSEP microcode will reside in the space not used by the baseline workstation. If additional space is needed, the display microcode can be overlayed during printer operation.

Diagnosability

O Dandelion includes very little hardware to support concepts like loopback. Some diagnostic aids will be added when the baseline system is in place and we can evaluate the marginal gain of any addition. Please remember that adding hardware to a system may improve diagnosability but it will in fact lower reliability.

Configuration Control

O Dandelion includes no system to automatically determine how it is configured. To the extent that we can add signal to tell when, for example, the Xerox Wire tranceiver is installed, we will do so on a case by case basis.